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Loretta S. Garcia

February 10, 2006

CUSTOMER NO. 36257

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Eliyahou HARARI et al.

Title: Flash EEPROM System

Application No.: 09/064,250

Filing Date: April 22, 1998

Examiner: Vu Anh LE

Group Art Unit: 2824

Docket No.: SNDK.006USM

Conf. No.: 5711

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application.

- ☒ According to 37 C.F.R. 1.98(2)(ii), copies of the U.S. Patents and U.S. Published Patent Applications documents are not required and are therefore not enclosed. Copies of the listed foreign patent documents or Other Art are enclosed.


Attorney Docket No.: SNDK.006USM

Application No.: 09/064,250

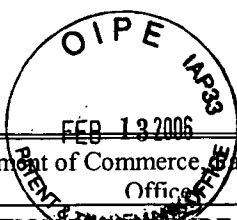
Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664. This form is being submitted in duplicate.

Respectfully submitted,

 February 10, 2006
Gerald P. Parsons Date
Reg. No. 24,486

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U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SN DK.006USM	09/064,250
(Use several sheets if necessary)	Applicant(s)	Conf. No.
(Form PTO-1449)	HARARI et al.	5711
	Filing Date	Group
	April 22, 1998	2824

U.S. Patent Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	4,090,258	05-1978	Cricchi			
	4,149,270	04-1979	Cricchi et al.			
	4,181,980	01-1980	McCoy			
	4,219,883	08-1980	Kobayashi et al.			
	4,253,059	02-1981	Bell et al.			
	4,272,830	06-1981	Moench			
	4,287,570	09-1981	Stark			
	4,393,475	07-1983	Kitagawa et al.			
	4,415,992	11-1983	Adlhoch			
	4,475,194	10-1984	LaValee et al.			

Foreign Patent Documents

							Translation	
	Document	Date	Country	Class	Subclass		Yes	No
	DE3637682	1987	Germany				abstract	
	DE3831538	1989	Germany				abstract	
	GB2061651	1981	United Kingdom					
	GB2029145	1980	United Kingdom					

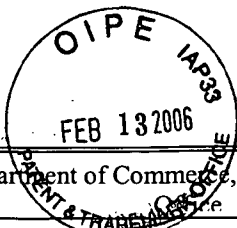
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	Alberts et al., "Multi-Bit Storage Fet Earom Cell", IBM Technical Disclosure Bulletin, Vol. 24, No.7A, Dec. 1981, pp. 3311-3314, 4193.
	Berenga et al. "E2-PROM TV Synthesizer", 1978 IEEE International Solid-State Circuits Conference: ISCCC 78", February 17, 1978, pp.196-197.
	"Bipolar /MOS Memories Data Book", <u>Advanced Micro Devices</u> , ISSN 0888-4714, pp.6-1-6-14, 1986
	Bleiker et al., "A Four State EEPROM Using Floating-Gate Memory Cells", IEEE Journal of Solid-State Circuits, Vol. Sc-22. No. 3, June 1987, pp.460-463.

Examiner /Vu Le/ Date Considered 01/30/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents

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	4,495,602	01-1985	Sheppard			
	4,586,163	04-1986	Koike			
	4,612,629	09-1986	Harari			
	4,677,590	06-1987	Arakawa			
	4,685,082	08-1987	Cheung			
	4,752,929	06-1988	Kantz			
	4,779,272	10-1988	Kohda et al.			
	4,799,195	01-1989	Iwahashi et al.			
	4,809,231	02-1989	Shannon et al.			
	4,847,808	07-1989	Kobatake			

Foreign Patent Documents

							Translation	
	Document	Date	Country	Class	Subclass		Yes	No
	JP5931158	1984	Japan				X	
	JP62188100	1987	Japan				abstract	
	JP0123878	1989	Japan					X
	JP0146949	1989	Japan					X

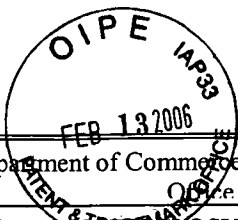
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	Caironi et al., "A TV Frequency Synthesis System With a Single Chip Microprocessor Interface Including Non-Volatile Memory", IEEE Transactions on Consumer Electronics, Vol. CE-28, No.3, pp.363-71, August 1982.
	Furuyama et al., "An Experimental 2-BIT/CELL Storage Dram for Macro Cell or Memory-on-Logic Application", IEEE Custom Integrated Circuits Conference, May 1988, pp. 4.4.1-4.4.4.
	Gee et al., "An Enhanced 16K E2PROM", IEEE Journal of Solid-State Circuits, Vol. SC-17, No.5, October 1982, pp. 828-832.
	Horiguchi et al. "An Experimental Large-Capacity Semiconductor File Memory Using 16-LEVEL/CELL storage", IEEE Journal of Solid-State Circuits, Vol. 23, Feb.1998, No.1, pp. 27-33.

Examiner /Vu Le/ Date Considered 01/30/2008

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U.S. Patent Documents

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	4,870,618	09-1989	Iwashita			
	4,943,962	07-1990	Imamiya et al.			
	4,956,816	07-1990	Atsumi et al.			
	4,959,812	09-1990	Momodomi et al.			
	4,980,861	12-1990	Herd et al.			
	4,939,690	07-1990	Momodomi et al.			
	4,996,669	02-1991	Endoh et al.			
	4,999,813	03-1991	Ohtsuka et al.			
	5,003,510	03-1991	Kamisaki			
	5,357,462	10-1994	Tanaka			
	5,361,227	01-1994	Tanaka et al.			
	5,602,987	02-1997	Harari et al.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	IBM Technical Disclosure Bulletin "EPROMgramming Device", Vol. 29, No.9, February 1987, pp. 4145-4146.
	Japanese Office Action (with translation), Application No. 123842/1999 for SanDisk Corporation, dated September 20, 2005, 5 pages.
	Krick, "Three-State MNOS FET Memory Array", IBM Technical Disclosure Bulletin, Vol. 18, No.12, May 1976, pp. 4192-4193.
	Kynett et al., "A 90-ns One Million Erase/Program Cycle 1-Mbit Flash Memory", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, October 1989, pp. 1259-1263.
	Kynett et al. "An In-System Reprogrammable 32K X 8 CMOS Flash Memory", IEEE Journal of Solid-State Circuits, Vol. 23, No.5, Log Number 8822443, October 1988, pp. 1157-1163
	Klingman, "Microprocessor Systems Design", Prentice-Hall, Inc. pp.30-31, 1977.

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INFORMATIONAL DISCLOSURE STATEMENT BY APPLICANT	SN DK.006USM	09/064,250
(Use several sheets if necessary)	Applicant(s)	Conf. No.
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U.S. Patent Documents

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	5,657,270	08-1997	Ohuchi et al.			
	5,793,696	08-1998	Tanaka et al.			
	5,831,903	11-1998	Ohuchi et al.			
	5,933,366	08-1999	Yoshikawa			
	6,014,327	01-2000	Banks			
	6,128,224	10-2000	Morton et al.			
	6,344,998	02-2002	Banks			
	6,356,486	03-2002	Banks			
	6,381,172	04-2002	Banks			
	6,404,675	06-2002	Banks			

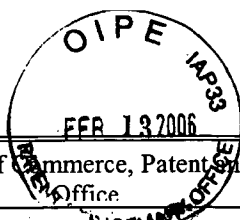
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	Masuoka et al. "A 256-KBIT Flash EEPROM Using Triple-Polysilicon Technology", IEEE Journal of Solid-State Circuits, Vol. SC-22, No.4, pp.548-552, New York, USA, August 1987.
	SGS-ATES "Excerpts From a 1983 Data Book", SGS-Ates Group, 45 pp., Nov. 1983.
	SGS-ATES. "PLL TV Microcomputer interface", SGA-ATES, MOS Integrated Circuits/M206, 15 pp. June 1982.
	Scrocchi et al. "EPM32-Electronic Program Memory System for TV (32 stations)" SGS-ATES, Technical Note#153, pp. 1-19, 1982.
	SEEQ Data Book 1988/89 SEEQ Technology, Inc. pp.3-1-3-7
	Stark, "Two Bits Per Cell ROM", Digest of Papers Spring COMCONS 81, Feb. 23-26, VLSI LABORATORY, pp. 209-212.
	Tanaka et al., "A 4-Mbit NAND-EEPROM with Tight Programmed Vt Distribution", 1990 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 105-106.

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	Torelli, "An LSI Technology Fully Compatible EAROM Cell", Component Electronic SpA, No. 6, Vol. LI, 7 pp. 1982.
	Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver in a Single Chip", IEEE Digest of Technical Papers, CAT. No.: 83CH1872-1, 2 pp., June 8, 1983
	Torelli et al., "Non-Volatile Station Memory and Remote-Control Receiver and Memory Display Driver", IEEE Transactions on Consumer Electronics, Vol. CE-29, No.3, pp.103-13, August 1983.
	Torelli et al., PLL2K-PLL Frequency Synthesizer for 30 Programs", SGS-ATES, Technical Note #152, pp.1-16, 1982.
	Torelli et al. "Single Chip, 16 Station TV Digital Tuning System", SGS Technical Note #170, pp.1-19, 1984.

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